1.1 kV 4H-SiC Power UMOSFET's

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***Abstract*—Silicon Carbide (4H-SiC), power UMOSFET's were fabricated and characterized from room temperature to 200 °C. The devices had a 12-μm thick lightly doped n-type drift layer, and a nominal channel length of 4 μm. When tested under Fluorinert™ at room temperature, blocking voltages ranged from 1.0 kV to 1.2 kV. Effective channel mobility ranged from 1.5 cm^2/V·s at room temperature with a gate bias of 32 V (3.5 MV/cm) up to 7 cm^2/V·s at 100 °C with an applied gate bias of 26 V (2.9 MV/cm). Specific on-resistance ($R_{on,sp}$) was calculated to be as low as 74 m$\Omega \cdot$cm^2 at 100 °C under the same gate bias.**

I. Introduction

RECENT SiC power device developments include 4.5 kV pn junction diodes, 1.75 kV Schottky diodes, 900 V thyristors, 700 V GTO's, and 760 V Double Implanted MOS (DIMOS) transistors [1]–[5]. SiC vertical power MOSFET devices are expected to have very low specific on resistance, fast switching, and outperform Si IGBT's in the 600–2000 V range. The 760 V power DIMOSFET's have a low specific on-resistance ($R_{on,sp}$ = 66 m$\Omega \cdot$cm^2) at an applied gate bias of 30 V (~6.25 MV/cm) [5], while other lower voltage (260 V) SiC UMOSFET's have reported extremely low on-resistance of 18 m$\Omega \cdot$cm^2 [3], [6] at an applied gate bias of 22 V (gate oxide thickness unreported). Most SiC MOS devices posses low blocking voltages because of high-temperature and high electric field stress on the gate oxides. Additional problems with the UMOS structure in SiC include poor oxide uniformity, higher interface state densities on the sidewall, electric field crowding at the trench corners, and Fowler–Nordheim (F–N) carrier injection across the gate oxide as a result of lower barrier heights for electron injection in the (4H-SiC)-SiO_2-polysilicon system [7], [8]. Despite technical challenges, the UMOS structure still offers inherent advantages over the DIMOS structure including smaller pitch and lower potential $R_{on,sp}$ due to the absence of the JFET region. Here, we report on a SiC UMOSFET capable of blocking up to 1.1 kV using a 12-μm thick drift layer.

II. Device Structure and Fabrication

A cross section of the 4H-SiC UMOSFET fabricated is shown in Fig. 1(a). A top view photograph of a 4H-SiC UMOS (13-μm pitch between fingers) is shown in Fig. 1(b), with gate and source/body contacts shown. The device structure was grown by vapor phase epitaxy on a heavily doped n-type, Si-face, 8° off-axis, 4H-SiC substrate. The 12-μm thick drift layer was doped with nitrogen (n-type) at ~1 × 10^{15} cm^{-3} as verified from capacitance-voltage measurements. Next, the p-type channel layer ($N_A \sim 7 \times 10^{16}$ cm^{-3}) was grown for a nominal channel length (L) of 4 μm. A common source and body contact was formed by implanting the n^+ source regions in channel layer and then implanting a p^+ region between the source regions. A common final metal connected source and body together, again see Fig. 1(b), with a top layer of gold used to facilitate gold-gold wirebonding. The gate trench and edge termination were both accomplished via reactive ion etching in CHF_3, H_2, and O_2. A combination of thermal and deposited silicon dioxide layers were used to passivate the mesa edge termination of the device. Extensive organic and chemical cleans [9], [10], as well as UV ozone cleaning to remove graphitic carbon from the surface, were performed prior to gate oxidation. A sacrificial oxide was grown prior to actual gate oxidation to smooth the trench corners (reduce field crowding) as well as consume damaged surface layers created by RIE. To minimize the difference in oxidation rates between the bottom and sides of the trench, the gate oxidation was done by growing a thin layer of thermal SiO_2 at 1150 °C in steam, followed by a low pressure chemical vapor deposition of SiO_2 to obtain a more uniform 90-nm thick gate oxide. Next, polysilicon gates were deposited and patterned to form the gate contact. Boron (p-type) doping of the polysilicon was used to diminish F–N tunneling through the gate oxide [8]. Nickel ohmic contacts were used for the drain and source/body. Interdigitated source and gate fingers were of equal lengths (250 μm) and widths for devices, although pitch varied from 13 to 38 μm. Smaller pitches of 6 to 10 μm have been suggested to increase charge sharing between neighboring cells [7], but the effects of pitch on device properties were not investigated here, but will be the subject of more detailed work to be presented later. The number of fingers ranged from 10 to 40 for the different cells. No edge termination techniques were employed in these devices.

III. Experimental Results and Discussion

Testing was performed on a high-temperature probe station in an air ambient with Fluorinert™. Specific contact resistivities were measured using TLM structures. Analysis of the n-type ohmic source TLM data revealed specific ohmic contact resistances of ~5–7 × 10^{-6} $\Omega \cdot$cm^2, while p-type body contacts had specific ohmic contact resistances of ~2–20 × 10^{-3} $\Omega \cdot$cm^2.

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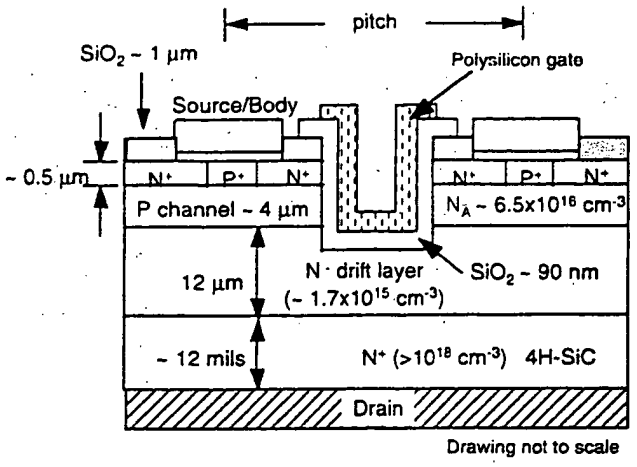
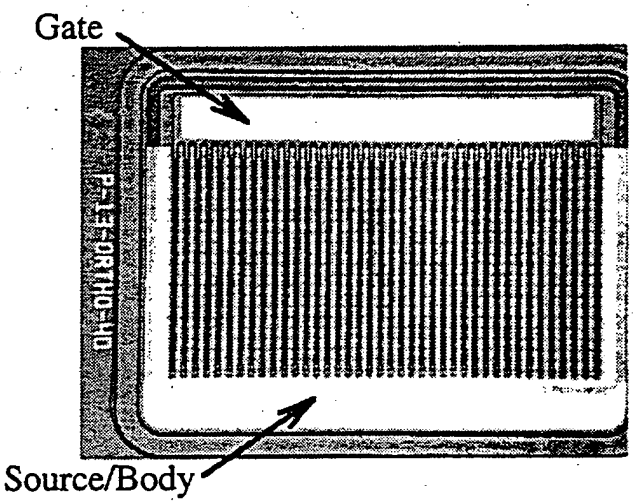


(a)



(b)

Fig. 1. 4H-SiC vertical UMOSFET (a) schematic device cross section and (b) top-view of a 13-μm pitch, 40-finger UMOS cell. Gate and source/body fingers shown with backside drain not shown. Gate length (L) was ~4 μm and trench width (W) was 20 mm.

Testing was performed using both a Tektronix 576 curve tracer, and computer-controlled Keithley 237 high-voltage source measurement units. Blocking voltages were measured from 1.0 to 1.2 kV. Forward $I-V$ characteristics of a 1.1 kV SiC UMOS (13-μm pitch, 10 fingers) are shown in Fig. 2. Maximum V_{DS} (1.1 kV) was limited by the Keithley 237. At 1.1 kV, the peak electric field at the pn junction is approximately 1 MV/cm calculated from abrupt one-side pn junction theory, and 2-D Pisces simulations of the device structure indicate that the field is enhanced as high as 1.6 MV/cm at the bottom trench corners. While placing other trenches in close proximity tends to reduce this field crowding [11], the values obtained here are comparable to the theoretical maximum electric field in SiC of ~2 MV/cm, especially considering that no edge termination was used, and that field crowding in the corners of the U trench also plays a significant role in premature gate oxide breakdown [7].

The effective electron channel mobility (μ) was low, consistent with that reported in other SiC power MOS devices [3], [6]. Values extracted from the linear region $I-V$ characteristics of a typical device ranged from 1.5 cm^2/V·s at room temperature with moderate applied gate bias (32 V or 3.5 MV/cm) and increased to 7 cm^2/V·s at 100 °C under 26 V (2.9 MV/cm) gate bias. The increase in μ with temperature is attributed to increased charge in the inversion layer as a result of electron emission from deeper level interface states, which has been reported elsewhere [10]. With V_{GS} of 26 V at

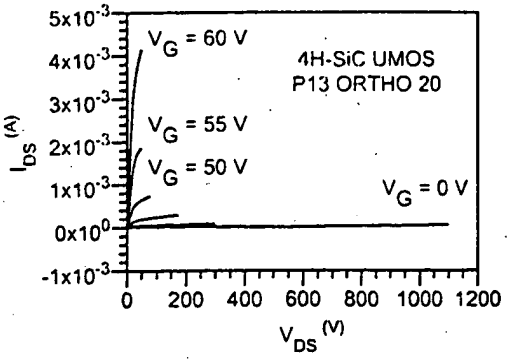


Fig. 2. Room temperature $I-V$ characteristics of a 1.1 kV 4H-SiC UMOSFET (13-μm pitch, 20 fingers, W = 10 mm) with 12-μm thick drift layer, measured with Fluorinert™.

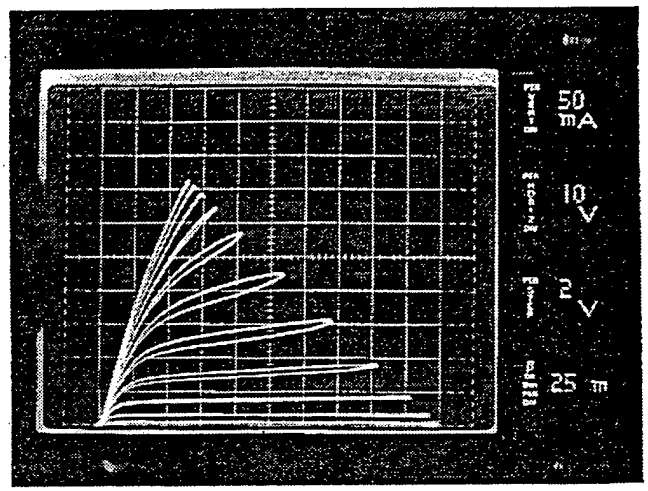


Fig. 3. $I-V$ characteristics of a 4H-SiC UMOSFET (16-μm pitch, 40 fingers, W = 20 mm, $L \approx 4\,\mu$m, and t_{ox} = 90 nm) at 100 °C. First trace corresponds to V_{GS} of 6 V, incremented in 2 V steps to a maximum V_{GS} of 26 V (2.9 MV/cm) with $R_{on,sp}$ of 74 mΩ·cm^2.

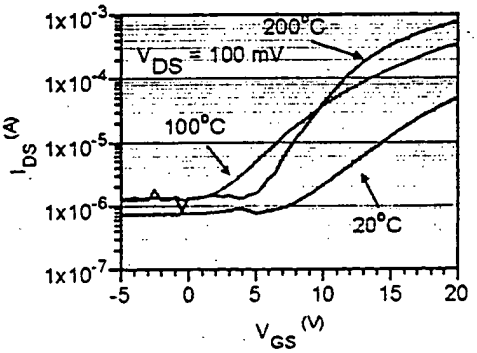


Fig. 4. Transfer characteristics of a 4H-SiC UMOSFET (16-μm pitch, 40 fingers, W = 20 mm) at 20, 100, and 200 °C in the linear region with V_{DS} = 100 mV. Gate bias was less than 20 V (2.2 MV/cm) at all times.

100 °C, this device had a forward voltage drop of 8.0 V at a current density of 108 A/cm^2, which is shown in Fig. 3. The corresponding $R_{on,sp}$ was 74 m$\Omega \cdot$cm^2 at this forward drop. While better performance could be obtained by increasing the gate bias to 6–10 MV/cm, these values would exceed the practical operating limit of gate bias for SiO_2 on SiC [7], [8]. Increased I_{DS} at higher temperatures is shown by the linear region (V_{DS} = 100 mV) transfer characteristics shown in Fig. 4 with gate bias <2.2 MV/cm, which is consistent with the measured increase in μ at higher temperature, and can be attributed to the poor oxide-SiC interface. Further study of this interface is necessary for improvement of these devices.

IV. Conclusion

4H-SiC UMOSFET's have been fabricated and characterized with measured room-temperature blocking voltages ranging from 1.0 kV to 1.2 kV as a result of proper device design and fabrication, including the use of stacked grown/deposited gate dielectric, boron-doped polysilicon for gate contact, and common source/body contacts used to reduce the finger pitch. Reducing the finger pitch of the cells increased the charge sharing between fingers allowing for higher breakdown voltage. Increasing channel mobility (from 1.5 cm^2/V$\cdot$s at room temperature and 7 cm^2/V$\cdot$s at 100 °C) by optimizing the SiC-SiO_2 interface was identified as a key task necessary to achieve optimal specific on-resistance. $R_{on,sp}$ was 74 m$\Omega \cdot$cm^2 with an applied gate bias of 2.9 MV/cm at 100 °C for these devices.

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References

[1] O. Kördina, J. P. Bergman, A. Henry, E. Janzen, S. Savage, J. Andr L. P. Ramberg, U. Lindefelt, W. Hermansson, and K. Bergman, "A 4. kV 6H-SiC rectifier," *Appl. Phys. Lett.*, vol. 67, pp. 1561–1563, 1995

[2] A. Itoh, T. Kimoto, and H. Matsunami, "Excellent reverse blockin characteristics of high-voltage 4H-SiC Schottky rectifiers with boror implanted edge termination," *IEEE Electron Device Lett.*, vol. 17, pp 139–141, Mar. 1996.

[3] J. W. Palmour, R. Singh, L. A. Lipkin, and D. G. Waltz, "4H-silico carbide high-temperature power devices," in *Trans. 3rd Int. Conf. High Temperature Electronics (HiTEC)*, 1996, vol. 2, pp. XVI-9–14.

[4] A. K. Agarwal, J. B. Casady, L. B. Rowland, W. F. Valek, and C. D Brandt, "700 V asymmetrical 4H-SiC gate turn-off (GTO) thyristors, *IEEE Electron Device Lett.*, vol. 18, pp. 518–521, Nov. 1997.

[5] J. N. Shenoy, J. A. Cooper Jr., and M. R. Melloch, "High-voltag double-implanted power MOSFET's in 6H-SiC," *IEEE Electron Devic. Lett.*, vol. 18, pp. 93–95, Mar. 1997.

[6] J. W. Palmour, S. T. Allen, R. Singh, L. A. Lipkin, and D. G. Waltz "4H-silicon carbide power switching devices," *Inst. Phys. Conf. Ser.* no. 142, pp. 813–816, 1996.

[7] A. K. Agarwal, R. R. Siergiej, S. Seshadri, M. H. White, P. G. McMullin A. A. Burk, L. B. Rowland, C. D. Brandt, and R. H. Hopkins, "Critica materials, device design, performance, and reliability issues in 4H-SiC power UMOSFET structures," in *Mater. Res. Soc. Symp. Proc.*, 1996 vol. 423, pp. 87–92.

[8] A. K. Agarwal, S. Seshadri, and L. B. Rowland, "Temperature depen dence of Fowler–Nordheim current in 6H and 4H SiC MOS capacitors,' *IEEE Electron Device Lett.*, this issue, pp. 592–594.

[9] J. N. Shenoy, G. L. Chindalore, M. R. Melloch, and J. A. Cooper Jr., "Characterization and optimization of the SiO_2/SiC metal-oxide-semiconductor interface," *J. Electron. Mater.*, vol. 24, no. 4, pp. 303–309, 1995.

[10] D. M. Brown, E. Downey, M. Ghezzo, J. Kretchmer, V. Krishnamurthy, W. Hennessy, and G. Michon, "Silicon carbide MOSFET technology," *Solid-State Electron.*, vol. 39, no. 11, pp. 1531–1542, Nov. 1996.

[11] T. P. Chow, private communication, Rensselaer Polytechnic Institute, Troy, NY.